Study on the Analytical Model of non-planar MOSFET

Munawar A Riyadi*, Darjat, Teguh Prakoso
Dept. of Electrical Engineering,
Diponegoro University
Semarang, Indonesia 50275
*e-mail : munawar@undip.ac.id

Jatmiko E. Suseno
Dept. of Physics,
Diponegoro University
Semarang, Indonesia 50275

***Abstract*— In the recent development of MOSFET, non-planar structure has been identified as promising structure for next device generation. The advanced scaling of device implies that more sophisticated model is required due to the limitation of the existing models for application in nano scale. Analytical model for non-planar MOSFET model is discussed in this paper, especially for device with pillar. The concern of channel shape and structure is elaborated as well. The result shows the shift in subthreshold characteristic due to the presence of recessed region in the channel with the simulated model.**

***Keywords*—non-planar MOSFET; nanoscale; analytical model; surface potential, short channel effect**

I. INTRODUCTION

The rapid progress of MOSFET into nanoscale dimension reveals the limited option for prolonging the conventional bulk structure legacy, as stated by the latest International Technology Roadmap for Semiconductor (ITRS)[1]. The continuous scaling of the device dimension has now reached tens of nanometer size especially for the channel length of transistors. Several innovations for future devices are emerged, mainly with non-conventional structure, which may overcome the problem of conventional MOSFET device in nanoscale. Such device is non-planar MOSFET with a variety of pillar stuctures, as noted by many researchers [2-8]. The advantages of non-planar MOSFET are due to the relaxed-lithography in defining the channel length and also on its ability to obtain self-aligned double gate for the structure; an advantage that is hard to produce in conventional one.

On the other hand, several distinct methods of fabrication result in different channel shape. Several techniques produce straight channel between source and drain, while some other produces channel in such a bending shape, a combination of vertical and recessed horizontal direction of current. Different channel potentials may exist due to the shape of source or drain as well. The recessed channel (Fig. 1(a)) has the L-shape geometry with the presence of corner that diverts the direction of current flux from drain to source. On the other hand, the body-tied geometry (Fig. 1(b)) offers the possibility of direct flux, but with the channel connected to the substrate potential. The other geometry, floating body channel (Fig. 1(c)), resembles the simple double gate structure, while the channel potential is isolated electrically from the substrate. All geometries may be found in non-planar double gate MOSFET.

Several models that simulate the physics of the vertical devices have been published recently. However, many authors focused on the ideal non-doped double-gate/surround gate MOSFET structure [9-11]. Others modeled the highly doped MOSFET with the help of regional model [12, 13] or depletion charge [14] as well as with conformal mapping [15]. However, the analytical model for non-ideal junction structure, as well as recessed channel, has not been well articulated in previous publications. In the conventional MOSFET, the recessed gate is known for its ability to prevent short channel effect, but in the vertical geometry, the recessed channel is somewhat different with that of conventional. The simulation of recessed gate in vertical MOSFET geometry has been presented in [16], but it is mainly concentrated for vertical surround gate, and no analytical model was offered.

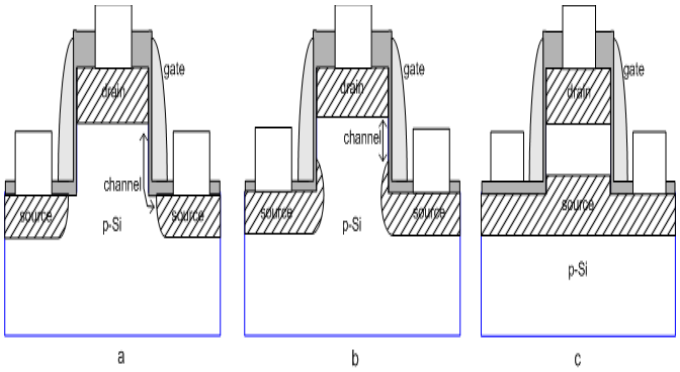

Fig. 1 The variation of channel geometry in non-planar DG MOSFET: (a) recessed, L-shape channel, (b) body-tied channel, and (c) floating-body channel

Therefore, in order to explain the behaviour of channel with different shape and potential profile, it is important to derive the appropriate model. In addition, the continuous scaling of device requires applicable model in nanoscale. This paper elaborates the analytical model of non-planar MOSFET which employ the recessed channel geometry in the bottom part. The corner effect is elaborated extensively,

with the help of approach that has been provided for conventional model[17].

II. DEVICE MODEL

The structure of recessed channel in non-planar MOSFET can be seen in Fig. 2. This typical structure is an ideal form of the fabricated devices. The straight channel potential model is derived from Poisson equation

$$\frac{d^2\psi(x,y)}{dx^2} + \frac{d^2\psi(x,y)}{dy^2} = \frac{qN_A}{\epsilon_{Si}} \quad (1)$$

using generic approach as noted in several references, e.g. [10, 18-21]. Moreover, the presence of corner region in the bottom is arguably difficult to solve using two-dimensional Poisson equation in Cartesian system. Therefore, we divide the channel into two regions: first is the straight and latter is the corner region. We simplify the corner region as a quarter circle, an approach adopted from Zhang et al [17] for grooved gate in conventional MOSFET. However, Zhang's model used trapezium-shape approach, while our model employs quarter-circle approach which is more realistic.

The uniformed depletion width x_d is calculated using the following formula:

$$x_d = \frac{D_A}{L} \quad (2)$$

D_A is the total depletion region area as in [22], as simplification of depletion width towards all area mainly due to the gate influence.

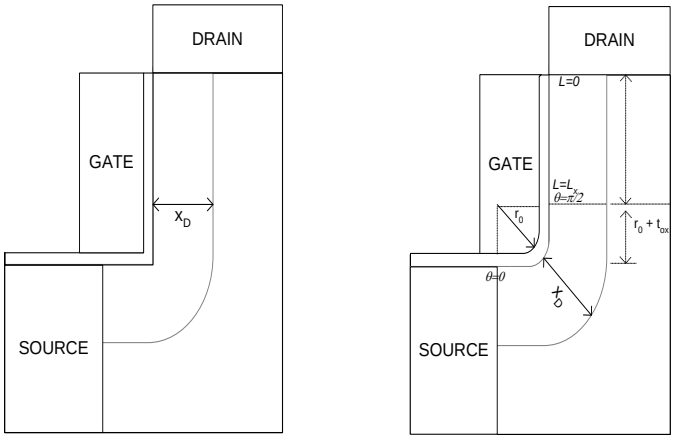

Fig. 2 The structure of recessed channel in vertical geometry (a), and its approach using two-region solution (b)

The potential of channel for each region is following the two dimensional second-order parabolic approach of graded channel approximation (GCA) that originally proposed by Young [23]. However, for corner area, the parabolic approximation is adopted to the cylindrical coordinate system as was used in [17]. The potential for both cartesian and polar coordinate systems are:

$$\psi_{st}(x,y) = \phi_s(x) + C_{11}(x)y + C_{12}(x)y^2 \quad (3)$$

$$\psi_{cr}(r,\theta) = C_{20}(\theta) + C_{21}r + C_{22}r^2 \quad (4)$$

The notation "*st"* stands for "straight", to differentiate with "*cr*" for "corner". In solving the differential Poisson equation using general parabolic approach, several boundary conditions are set, which are applied to both regions (for polar coordinate, *x* and *y* should be replaced with θ and r, respectively):

(i) The electric field in the silicon-oxide interface is according to Gauss' law [22]:

$$-\frac{\partial\psi_s}{\partial y}\Big|_{y=0} = \frac{C_{ox}}{\epsilon_{Si}}(V_{gn} - \phi_s(x)) \quad (5)$$

(ii) The potential at depletion layer is equal to the substrate potential, for body-tied channel to the V_{sub} :

$$\psi_s(x, x_d) = V_{sub} \quad (6)$$

(iii) The electric field in the depletion layer is:

$$\frac{\partial\psi}{\partial y}\Big|_{y=x_d} = 0 \quad (7)$$

All parameters are put and later the potential equation is rewritten as:

$$\psi_{st}(x,y) = \frac{V_{sub}y^2}{{x_d}^2} - \frac{V_{g1}y\epsilon_{ox}}{t_{ox}\epsilon_{si}} + \frac{V_{g1}y^2\epsilon_{ox}}{t_{ox}x_d\epsilon_{si}}$$

$$+\left(1 - \frac{y^2}{{x_d}^2} + \frac{y\epsilon_{ox}}{t_{ox}\epsilon_{si}} - \frac{y^2\epsilon_{ox}}{t_{ox}x_d\epsilon_{si}}\right)\phi_{s1}(x) \quad (8)$$

Similarly for the corner area, with inner radius $r_0 = L_{lateral} - t_{ox}$, depletion depth $r_d = r_0 + t_{ox} + x_d$ and capacitance of cylindrical tube $C_{ox} = \epsilon_{ox}/(r_0 \ln[1 + t_{ox}/r_0])$ as derived in [24], by borrowing quarter circle approach of grooved channel, solving all boundary conditions for corner area's potential result in [17]:

$$\psi_{cr}(r,\theta) = V_{sub} - M\left(\frac{r^2 - 2r(r_0+t_{ox}+x_d) + (r_0+t_{ox}+x_d)^2}{2r_0x_d}\right) * \left(V_{g1} - \varphi_{s2}(\theta)\right) \quad (9)$$

where $M = \frac{\epsilon_{ox}}{\epsilon_{si}}\,(1/\mathrm{Ln}[1 + t_{ox}/r_0])$.

Eq. 9 shows that the potential equation throughout the corner are dependent of r_0, which represent the length of recessive part of the channel. By substituting potential equation $\psi_{st}(x,y)$ of Eq. 8 back into Poisson's equation, a differential equation of potential in straight channel is obtained:

$$\frac{qN_A}{\epsilon_{si}} = \frac{2V_{sub}}{{x_d}^2} + \frac{2V_{g1}\epsilon_{ox}}{t_{ox}x_d\epsilon_{si}} - \frac{2(x_d\epsilon_{ox}+t_{ox}\epsilon_{si})}{t_{ox}{x_d}^2\epsilon_{si}}\phi_{s1}(x) + \frac{(x_d-y)(x_d y\epsilon_{ox}+t_{ox}(x_d+y)\epsilon_{si})}{t_{ox}{x_d}^2\epsilon_{si}}\phi_{s1}''(x) \quad (10)$$

Similarly for corner area, the surface potential $\varphi_{s2}(\theta)$ of Eq. 9 is substituted into Poisson's equation for polar coordinate [17]:

$$\frac{d^2\psi}{dr^2} + \frac{1}{r}\frac{d\psi}{dr} + \frac{1}{r^2}\frac{d^2\psi}{d\theta^2} = \frac{qN_A}{\epsilon_{Si}} \quad (11)$$

which result in [17]

$$\frac{V_{g1}-\varphi_{s2}(\theta)}{{\lambda_2}^2} + \varphi_{s2}''(\theta) = \frac{qN_A}{\epsilon_{si}}\frac{(r_0+t_{ox})x_d}{{\lambda_2}^2 M(r_0+t_{ox}-x_d)} \quad (12)$$

It is noteworthy that Poisson equation of both regions as expressed in Eqs. 10 and 12 can be rearranged in the generic second-order differential equation formula [25] which has the common form of:

$$\phi_{s1}''(x) - \frac{\phi_{s1}(x)}{{\lambda_1}^2} = \beta_1 \text{ , (straight)} \quad (13)$$

$$\varphi_{s2}''(\theta) - \frac{\varphi_{s2}(\theta)}{{\lambda_2}^2} = \beta_2 \text{ , (corner)} \quad (14)$$

The boundary conditions for both regions can be ascribed as:

i. $\psi_{st}(0,0) = \phi_{s1}(0) = V_{bi} + V_{ds}$

ii. $\psi_{st}(L_x,0) = \phi_{s1}(L_x) = V_p = \varphi_{s2}(0)$

iii. $\varphi_{s2}(\pi/2) = V_{bi} + V_{sub}$

iv. $$\left.\frac{\partial\phi_{s1}}{\partial x}\right|_{x=L_x} = \left.\frac{\partial\varphi_{s2}}{r\partial\theta}\right|_{\theta=0} \quad (15)$$

Threshold voltage V_T is determined when the value of minimum surface potential is twice the Fermi potential $\varphi_{s,min} = 2\phi_F$. Thus, the location of the minimum potential along the surface in the channel obeys the expression:

$$\left.\frac{\partial\phi_s}{\partial x}\right|_{x=x_{min}} = 0 \quad (16)$$

By solving the boundary conditions and calculating the location of minimum potential in each regions, the threshold voltage can be determined from the minima of both regions.

III. RESULT AND DISCUSSION

The structure of straight channel with no corner effect is simulated in the similar way of the recessed structure. In the body-tied structure, the body of channel outside the depletion region is tied to the potential of substrate, V_{sub}. The surface potential of recessed and non-recessed channel are shown in Fig. 3 as a function of channel length for a fixed recessed length, L_{rec}=10 nm. Meanwhile, Fig. 4 shows the surface potential with the recessed channel is limited to around 15% of the total channel length L. It is notable that the minimum surface potential is located in the straight region for L_{rec} < 40% L.

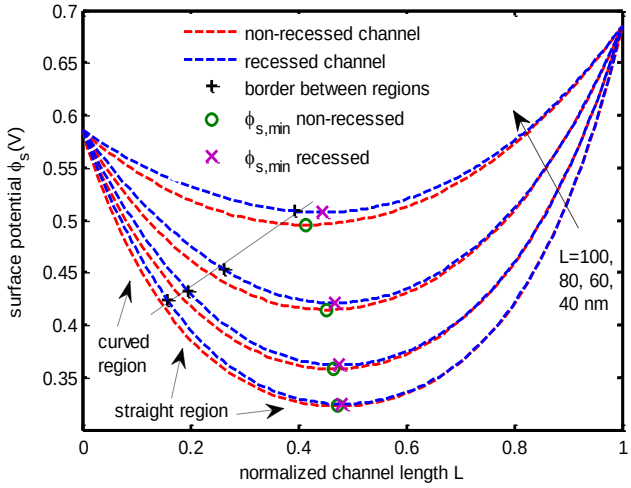

Fig. 3 The surface potential for recessed and non-recessed channel. the length recessed part are constant (10 nm), V_{ds}=0.1 V. t_{ox} = 3 nm, V_{gs}=0.1V

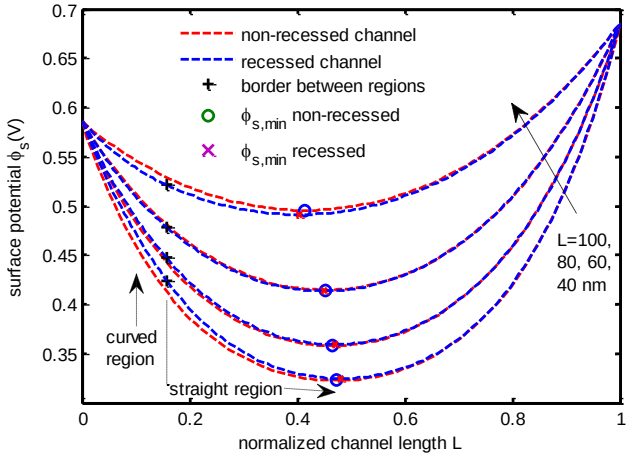

Fig. 4 The surface potential as a function of normalized channel length, with the recessed region length are 15% of L. V_{ds}=0.1 V. t_{ox} = 3 nm, V_{gs}=0.1V

The threshold voltage extraction is shown in Fig. 5 for L_{rec} = 15% L, V_{ds}=0.1 V, N_A= 10^{18} cm^{-3}, t_{ox}=2 nm. The threshold voltage is decreased in shorter channel. The straight channel has lower threshold voltage than the recessed channel. In an environment of low V_{DD}, as in low-power nano IC, lower threshold voltage is preferable, for a safe switching and higher current at on state.

Physically, the curved channel structure lacked the gate control in the corner region. The similar phenomenon is also found in grooved channel in planar MOSFET, as has been elaborated in [26, 27]. The lack of gate control produces decreased potential in the corner area compared to the straight channel. It also prevents the quick conversion into inversion in the channel beneath the oxide layer, with the

charge slowly respond to the gate voltage. As a result, higher threshold voltage is needed in the recessed channel.

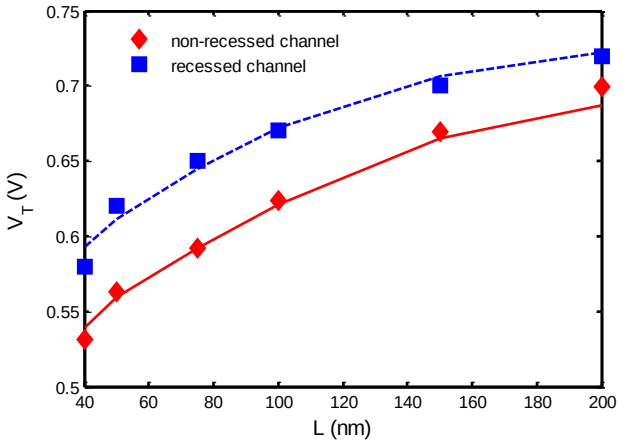

Fig. 5 The threshold voltage due to short channel effect.

IV. Conclusion

The structure of non-planar MOSFET with recessed channel has been modeled analytically using parabolic approach, with the help of two distict region representing different channel shape. The model successfully reveals the performance in the presence of short channel effect. The simulation based on the developed model shows the shift of threshold voltage due to the presence of the recessed part in the corner. The result reveals the implication of the usage of pillar for non-planar structure, which requires more careful design in the future for threshold-sensitive application .

Acknowledgment

The authors express their gratitude to LP2M (Diponegoro University) and DIKTI for the financial support under BOPTN-Fundamental Grant scheme. The authors also thank Prof. Razali Ismail of Universiti Teknologi Malaysia, for the fruitful discussion and the supporting research environment for parts of the research.

References

[1] *International Technology Roadmap for Semiconductors (ITRS) - 2009*. Available: http://www.itrs.net/reports.html

[2] T. Endoh, *et al.*, "Sub-10 nm Multi-Nano-Pillar Type Vertical MOSFET," *IEICE Transactions on Electronics*, vol. E93-C, pp. 557-562, 2010.

[3] A. Sugimura, *et al.*, "Proposal of Vertical-Channel Metal Oxide Semiconductor Field-Effect Transistor with Entirely Oxidized Silicon Beam Isolation," *Japanese Journal of Applied Physics*, vol. 48, Apr 2009.

[4] M. A. Riyadi, *et al.*, "Vertical Double Gate MOSFET For Nanoscale Device With Fully Depleted Feature," *AIP Conference Proceedings*, vol. 1136, pp. 248-252, 2009.

[5] J. Pan, "The Gate-Controlled Diode, High-Frequency, and Quasi-Static C-V Techniques for Characterizing Advanced Vertical Trenched Power MOSFETs," *IEEE Transactions on Electron Devices*, vol. 56, pp. 1351-1354, Jun 2009.

[6] M. Masahara, *et al.*, "Vertical Ultrathin-channel Multi-gate MOSFETs (MuGFETs): Technological Challenges and Future Developments," *IEEJ Transactions on Electrical and Electronic Engineering*, vol. 4, pp. 386-391, May 2009.

[7] L. Tan, *et al.*, "The influence of junction depth on short channel effects in vertical sidewall MOSFETs," *Solid-State Electronics*, vol. 52, pp. 1002-1007, 2008.

[8] J. Moers, "Turning the world vertical: MOSFETs with current flow perpendicular to the wafer surface," *Applied Physics A: Materials Science & Processing*, vol. 87, pp. 531-537, 2007.

[9] Y. Taur, *et al.*, "A continuous, analytic drain-current model for DG MOSFETs," *IEEE Electron Device Letters*, vol. 25, pp. 107-109, 2004.

[10] Y. Taur, "An analytical solution to a double-gate MOSFET with undoped body," *IEEE Electron Device Letters*, vol. 21, pp. 245-247, 2000.

[11] X. P. Liang and Y. Taur, "A 2-D analytical solution for SCEs in DG MOSFETs," *IEEE Transactions on Electron Devices*, vol. 51, pp. 1385-1391, Sep 2004.

[12] J. He, *et al.*, "A continuous analytic channel potential solution to doped symmetric double-gate MOSFETs from the accumulation to the strong-inversion region," *Chinese Physics B* vol. 20, Jan 2011.

[13] K. Chandrasekaran, *et al.*, "Compact modeling of doped symmetric DG MOSFETs with regional approach," in *Workshop on Compact Modeling, NSTI-Nanotech*, MA, USA, 2006, pp. 792 - 795.

[14] D. Munteanu, *et al.*, "Compact model of the quantum short-channel threshold voltage in symmetric Double-Gate MOSFET," *Molecular Simulation* vol. 31, pp. 831-837, Oct 2005.

[15] S. Kolberg and T. A. Fjeldly, "2D Modeling of nanoscale DG SOI MOSFETs in and near the subthreshold regime," *Journal of Computational Electronics* vol. 5, pp. 217-222, 2006.

[16] B. Subrahmanyam and M. J. Kumar, "Recessed source concept in nanoscale vertical surrounding gate (VSG) MOSFETs for controlling short-channel effects," *Physica E-Low-Dimensional Systems & Nanostructures*, vol. 41, pp. 671-676, Feb 2009.

[17] X.-J. Zhang, *et al.*, "Analytical analysis of surface potential for grooved-gate MOSFET," *Chinese Physics*, vol. 15, pp. 631-635, 2006.

[18] Z. Ghoggali and F. Djeffal, "Analytical analysis of nanoscale fully depleted Double-Gate MOSFETs including the hot-carrier degradation effects," *International Journal of Electronics*, vol. 97, pp. 119-127, 2010.

[19] F. Djeffal, *et al.*, "Analytical analysis of nanoscale multiple gate MOSFETs including effects of hot-carrier induced interface charges," *Microelectronics Reliability*, vol. 49, pp. 377-381, 2009.

[20] H. Lu and Y. Taur, "An analytic potential model for symmetric and asymmetric DG MOSFETs," *IEEE Transactions on Electron Devices*, vol. 53, pp. 1161-1168, 2006.

[21] B. Yu, *et al.*, "Explicit Continuous Models for Double-Gate and Surrounding-Gate MOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, pp. 2715-2722, 2007.

[22] V. Venkataraman and S. Nawal, "Modeling and Simulation of Strained Silicon MOSFETs for Nanoscale Applications," Bachelor of Technology dissertation, Department of Electrical Engineering, Indian Institute of Technology Delhi, Delhi, 2006.

[23] K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 36, pp. 399-402, 1989.

[24] X. Zhang, *et al.*, "An Analytical Model for Threshold Voltage of Grooved-Gate MOSFET's [in Chinese]," *Chinese Journal of Semiconductors*, vol. 4, pp. 441-445, 2004.

[25] E. Kreyszig, *Advanced engineering mathematics*, 9th ed.: Wiley, 2006.

[26] B. Doris, *et al.*, "Extreme scaling with ultra-thin Si channel MOSFETs," *Electron Devices Meeting, 2002. IEDM'02. Digest. International*, pp. 267-270, 2002.

[27] J. Tanaka, *et al.*, "A sub-0.1μm grooved gate MOSFET with high immunity to short-channel effects," in *Electron Devices Meeting, 1993. IEDM '93. Technical Digest., International*, 1993, pp. 537-540.