Bulletin of Electrical Engineering and Informatics
Vol. 8, No. 3, September 2019, pp. 798~807
ISSN: 2302-9285, DOI: 10.11591/eei.v8i3.1526

Parasitic consideration for differential capacitive sensor

Nurul Arfah Che Mustapha, A. H. M. Zahirul Alam, Sheroz Khan, Amelia Wong Azman
Department of Electrical and Computer Engineering, International Islamic University Malaysia, Malaysia

Article Info

Article history:

Received Mar 10, 2019
Revised May 12, 2019
Accepted May 27, 2019

Keywords:

CVC
Differential capacitive sensing
Parasitic impedance
Results improvement
Sensor sensitivity

ABSTRACT

Parasitic integration for a single supply differential capacitive sensing technique is presented in this paper. In real capacitive sensor measurement, parasitic impedance **exists** in its measurement. This paper objective is to study the effect of capacitive and resistive parasitic to the capacitive sensor circuit. The differential capacitive sensor circuit derivation theory is elaborated first. Then, comparison is made using simulation. Test was carried out using frequency from 40 kHz up to 400 kHz. Result is presented and have shown good linearity of 0.99984 at 300 kHz, R-squared value. This capacitive sensor is expected to be used for energy harvesting application.

Corresponding Author:

Nurul Arfah Che Mustapha,
Department of Electrical and Computer Engineering,
International Islamic University Malaysia,
P.O. Box 10, Jalan Gombak, 50728 Kuala Lumpur, Malaysia.
Email: nurularfah@iium.edu.my

1. INTRODUCTION

In instrumentation and measurement research field, capacitive sensor measuring system easily provides efficient changes of parameter of interest into various range of capacitance conversion. Such advantage takes place without functionality loss compared to resistive and inductive sensors [1]. Capacitive sensor uses electric field to sense either conductive or non-conductive material, as long the material has surface area, its dielectric material and within the electric field distance [2]. The design of capacitive sensors can be categorized into several requirements. Such requirements are shown in works that require accuracy [3], resolution [4], noise immunity [5] and sensitivity [6].

Due to its low power consumption and its sensing element consumes no energy, capacitive transducer sensor could be a contribution factor for low power measurement. There have been great efforts on the readout circuit and several reported ways of conversion using capacitance sensing for sensor interface circuits. Before capacitance conversion takes place into other forms like frequency, phase or digital, it first converts into voltages and continue its conversion process into desired forms depending on the design and method used in the system.

Majority of previous work utilizing the differential capacitive sensing presented based on operational amplifiers [7-8]. This work is an extended version of work in [6] that will discuss on its parasitic consideration in real application. The supply used in this circuit is a single source that provide its power to the discrete components circuits, such as oscillator, operational amplifiers, voltage divider circuit and instrumentation amplifier. It was tested that using this method frequency 40 kHz up to 400 kHz are suitable to be used in the system. However, focus of this paper is on frequency at 300 kHz.

2. RESEARCH METHOD

One of the important consideration should be included in real circuit are parasitic capacitance and resistance associated at the capacitance sensor. This is usually caused by connecting wires and circuit construction. The total parasitic capacitance and resistances are often contributing to error in measurement from the actual reading and may reduce the sensitivity level of the system if not properly managed.

2.1. Parasitic capacitance and resistance theory

In actual setting, based on work proposed in [6], there are also parasitic capacitance, C_{p1} and C_{p2} at capacitance sensor, C_x which is located at on one side of the C_x electrode, parallel to the excitation sinusoidal source and parallel to the noninverting amplifier input, respectively. The third parasitic capacitor, C_{p3}, which is found at the offset capacitor parallel to the C_x can be cancelled by nulling the capacitor or offset nulling through differential capacitance sensing, as confirmed in [5, 9-10]. These parasitic capacitance and resistances are shown in Figure 1. The proposed differential capacitive sensor is based on Figure 2 of [6] and [11]. This figure is not included in this paper due to avoid repetitive publication.

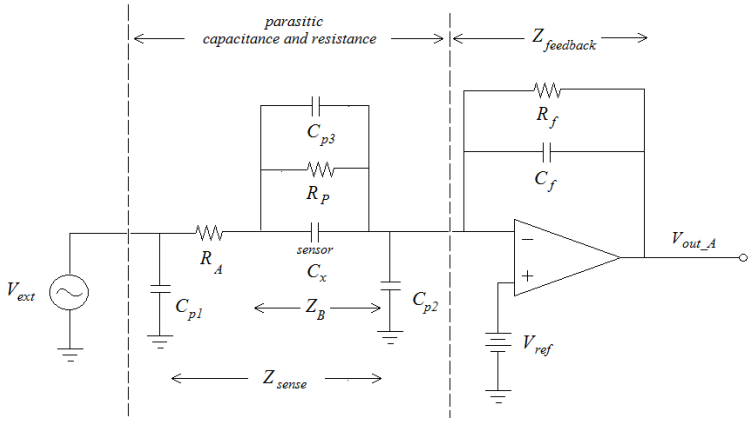

Figure 1. Half of the differential capacitance sensing circuit with parasitic

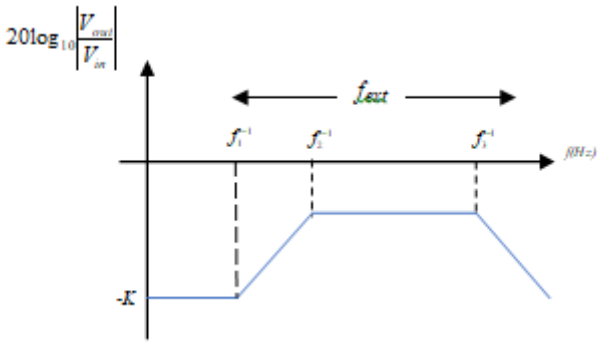

Figure 2. Estimated bode plot of V_{out_A}/V_{in} from the theory

In this case, capacitive sensor, C_x electrodes need to be properly shielded in order to give actual measurement and to avoid environment electromagnetic interference that would affect the behaviour of the circuit. However, in real situation stray capacitance always form between the shielding and the electrodes even in fully shielded condition.

Due to this, proper handling on the contributed parasitic resistance and capacitances should be taken into account. Theoretically, parasitic capacitance, C_{p1} and C_{p2}, have virtually no effect on the current passing through C_x when measurement is taken from the sensor capacitor, C_x. This is due to the low ohmic of the input voltage excitation signal at one side of the electrodes and C_{p2} is negligible because of low impedance value at the input amplifier.

The excitation voltage, $V_{ext}\cos(2\pi f_{ext}t+\varphi)$, with an amplitude voltage, V_{ext}, excitation frequency, f_{ext}, and φ is the magnitude phase angle. Z_B is an equivalent impedance at the sensor capacitance, C_x, where the parasitic resistance, R_p, and parasitic capacitance, C_{p3}, are in parallel to the sensor. $Z_{feedback}$ is the equivalent impedance at the sensing Opamp. Note that in this writing, the discussion only focus on one side of the differential Capacitance-to-Voltage Converter (CVC), since the other half behave the same as long as the components value is kept identical in symmetrical order. The transfer function derivation of circuit in Figure 1 are given in (1) to (3)

$$Z_{sense}=R_A+Z_B=R_A+\frac{R_P}{j\omega R_P(C_x+C_P)+1}=\frac{j\omega R_AR_P(C_x+C_P)+R_A+R_P}{j\omega R_P(C_x+C_P)+1} \quad (1)$$

$$Z_{feedback}=\frac{R_f}{1+j\omega R_fC_f} \quad (2)$$

$$V_{out\_A}=\left(1+\frac{Z_{feedback}}{Z_{sense}}\right)V_{ref}-\frac{Z_{feedback}}{Z_{sense}}V_{ext} \quad (3)$$

2.2. The proposed conditions exist in real situation

This transfer function is independent of parasitic resistors as long as it is within the passband frequencies. By substituting (1) and (2) into (3), the transfer function of V_{out_A} is extended from [12] as in the following:

$$\begin{aligned}V_{out\_A}=&\left(1+\frac{R_f}{R_A+R_P}\left(\frac{1+j\omega R_P(C_x+C_P)}{(1+j\omega R_fC_f)\left(1+j\omega\frac{R_AR_P}{R_A+R_P}(C_x+C_P)\right)}\right)\right)V_{ref}\\&-\frac{R_f}{R_A+R_P}\left(\frac{1+j\omega R_P(C_x+C_P)}{(1+j\omega R_fC_f)\left(1+j\omega\frac{R_AR_P}{R_A+R_P}(C_x+C_P)\right)}\right)V_{ext}\\=&V_{ref}+\left(\frac{R_f}{R_A+R_P}\left(\frac{1+j\omega R_P(C_x+C_P)}{(1+j\omega R_fC_f)\left(1+j\omega\frac{R_AR_P}{R_A+R_P}(C_x+C_P)\right)}\right)\right)(V_{ref}-V_{ext})\end{aligned} \quad (4)$$

The target of CVC system is to have an independent and single source, i.e. from ambient energy, free from other additional sources, such as the battery. Due to the requirement, reference DC voltage source needs to be taken care of. Here, the value of the reference voltage, V_{ref}, which to be supplied to the non-inverting Opamp input is obtained through voltage divider circuit supplied by the energy harvested source, V_s. The reference voltage, V_{ref}, is set at half of source voltage, V_s, in order to gain a non-zero level output voltage at the end output voltage. This is due to the fact that any negative sides of sinusoidal wave will be cut out after rectification at the rectifier circuit (please refer to Figure 2 of [6]). Therefore, it is chosen to have the output voltage to be shifted at the half of V_s, which is at the reference voltage, V_{ref}.

As mentioned earlier, the supply voltage, V_s is obtained from ambient energy. Energy for V_{ref} is by choice is kept constant. However, because the source to this V_{ref} is supplied by supply voltage, V_s, received from available ambient sources. It should worth to consider certain cases may happen, i.e. decreasing in supply voltage from intended voltage level. Further effect can be studied on (4) by simplifying the equation to (5) to study the inconsistent V_{ref} voltage value conditions that may exist in the circuit.

$$V_{out\_A}=(1+A)V_{ref}-(A)V_{ext} \quad (5)$$

where

$$A = \frac{R_f}{R_A + R_P}\left(\frac{1 + j\omega R_P(C_x + C_P)}{\left(1 + j\omega R_f C_f\right)\left(1 + j\omega \frac{R_A R_P}{R_A + R_P}(C_x + C_P)\right)}\right) \quad (6)$$

It can be seen in (5) the output voltage includes V_{ref} and excitation voltage, V_{ext}, in its output value, V_{out_A}. The output voltage is categorised into several cases: (i) V_{ref}=0 (ii) $V_{ref} < V_{ext}$ (iii) V_{ref}=V_{ext} and (iv) $V_{ref} > V_{ext}$ as supported in [13]. The transfer function equations are derived as in (3.13) to (3.16)

Case I: V_{ref}=*0*

$$\left|\frac{V_{out\_A}}{V_{ext}}\right| = -A \quad (7)$$

Case II: $V_{ref} < V_{ext}$ when V_{ref}=(1 - *m*)V_{ext} where (*0* < *m* < *1*)

$$\left|\frac{V_{out\_A}}{V_{ext}}\right| = (1 + A)(1 - m) - A \quad (8)$$

Case III: V_{ref}=V_{ext}

$$\left|\frac{V_{out\_A}}{V_{ext}}\right| = 1 \quad (9)$$

Case IV: $V_{ref} > V_{ext}$ when V_{ref}=*n*V_{ext} where (*n* > *1*)

$$\left|\frac{V_{out\_A}}{V_{ext}}\right| = n + (n - 1)A \quad (10)$$

where *m* and *n* is the multiplier numbers of excitation input voltage, V_{ext} equal to (1-*m*)V_{ext} or *n*V_{ext}.

As long the excitation frequency satisfies the condition of within the cutoff frequencies boundary conditions imposed by the parasitic resistances, the frequency of input voltage is independent to the CVC system. The cutoff frequencies are:

$$f_{ext} \geq \frac{1}{j\omega R_f C_f} \quad (11)$$

$$f_{ext} \geq \frac{1}{j\omega R_P(C_x + C_P)} \quad (12)$$

$$f_{ext} \leq \frac{R_A + R_P}{j\omega R_A R_P(C_x + C_P)} \quad (13)$$

Several conditions may exist to the output voltage, one of it is when V_{ref}=*0*, the transfer function of $\left|\frac{V_{out\_A}}{V_{ext}}\right| = -A$, is further derived to obtain the estimated output voltage frequency range. This is shown in bode plot in Figure 2 where component values are as derived in (14)

$$K\frac{f_1}{f_2\cdot f_3}\frac{1+\frac{s}{f_1^{-1}}}{\left(1+\frac{s}{f_2^{-1}}\right)\left(1+\frac{s}{f_3^{-1}}\right)} \tag{14}$$

where

$$f_1 = R_P\left(C_x + C_P\right)$$
$$f_2 = R_f C_f$$
$$f_3 = \frac{R_A R_P}{R_A + R_P}\left(C_x + C_P\right) \tag{15}$$
$$K = -\frac{R_f}{R_A + R_P}\frac{R_P\left(C_x + C_P\right)}{R_f C_f \cdot \frac{R_A R_P}{R_A + R_P}\left(C_x + C_P\right)}$$

3. PARASITIC CAPACITANCE AND RESISTANCE INTEGRATION SIMULATION RESULTS

The simulation is done using OrCAD Capture Cadence 18.0 PSpice simulation. When V_{ref}=0, using components C_f=C_r=C_{x0}=5 *p*F and R_f=10 *M*Ω, C_x=8 *p*F and parasitic resistance R_A=20 *M*Ω, and R_P=2.2 Ω parasitic capacitance, C_P=5.6 *p*F. From Figure 2 and (14), expected corner frequencies from calculation in (11), (12) and (13), are 751 Hz, 3.18 *k*Hz and 6.82 *G*Hz, respectively as shown in the results of Figure 3. This shows a match simulation with the estimated theoretical drawing and values.

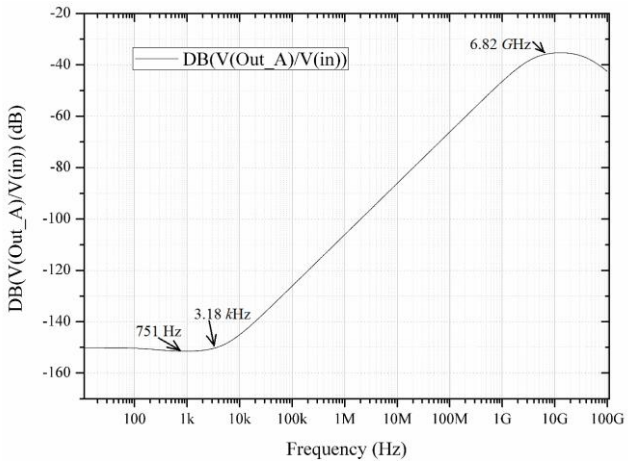

Figure 3. Simulated magnitude at opamp a output with parasitic

Further analysis of the overall transfer function for second condition when $V_{ref} < V_{ext}$ the transfer function is $\left|\frac{V_{out\_A}}{V_{ext}}\right| = (1+A)(1-m) - A$. Simulation result with integration of parasitic resistance and capacitance is shown in Figure 4. Expected corner frequencies from calculation in (11), (12) and (13), are 159, 588 Hz and 31.9 *k*Hz using components C_f=C_r=C_{x0}=5 *p*F and R_f=1 *M*Ω, C_x=8 *p*F and parasitic resistance R_A=20 *M*Ω, and R_P=2.2 Ω parasitic capacitance, C_P=5.6 *p*F.

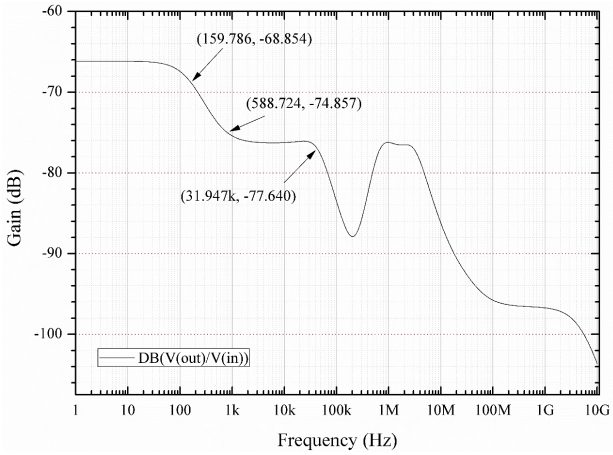

Figure 4. Simulated magnitude transfer function at the output CVC circuit.

3.1. Simulation of output voltage without parasitic integration

The linearity graph across frequencies obtained using R_f=10 *M*Ω, R_d=100 kΩ and C_d=0.1 μF, have shown wider detection range and high in sensitivity when run less than and equal to f_{ext}=100 *k*Hz. However, when frequency goes higher than 100 *k*Hz, which is shown in Figure 5, less points of detection is observed, and the sensitivity is low.

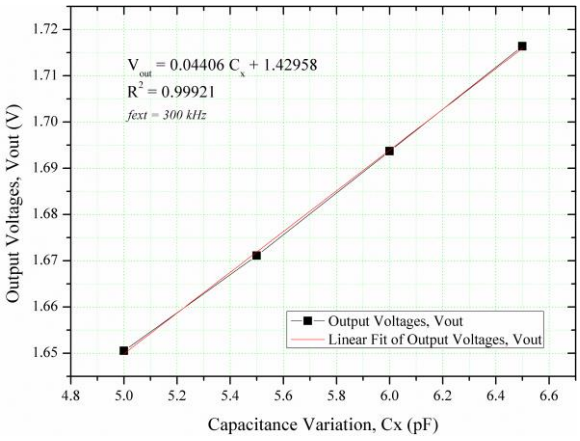

Figure 5. Effect of output voltage with C_x variation for R_d=100 *k*Ω and C_d=0.1 μF using V_s=3.3 V at 300 *k*Hz

By rules, the f_{-3dB} should be low than the cutoff frequency (f_c=3.18 *k*Hz). In this case has satisfied the condition when using R_d=100 *k*Ω and C_d=0.1 μF, the f_{-3dB}=15.9 Hz. Improvement on the number of detection points across certain capacitance range is increased by increasing the bandwidth of the low pass filter. This is by decreasing the R_d value and C_d value of the components. Figure 6 shows the simulation results using low R_d and C_d values of 10 *k*Ω and 0.01 μF respectively, with R_f=10 *M*Ω. In this case, the cutoff frequency, f_{-3dB}=1.59 *k*Hz, which satisfy the condition less than cutoff frequency f_c=3.183 *k*Hz.

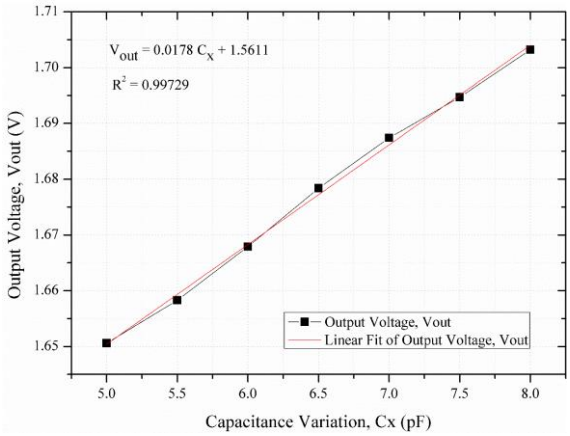

Figure 6. Effect of output voltage with C_x variation for R_d=10 *k*Ω and C_d=0.01 μF using V_s=3.3 V at 300 *k*Hz

The same trend is observed when frequency is increased, the detection capacitance is minimized. Compare to the previous results of Figure 5, the differential CVC output voltage is improved by more points were detected across wider capacitance range, using same capacitance change, ΔC_x=0.5 *p*F as seen in Figure 6. This method is suitable if high frequency of operation is targeted over the sensitivity, due to low sensitivity is observed at high frequency.

Improvement is made to the capacitance change, ΔC_x so that wider capacitance range is been detected with low detection change at high frequency. This is done by using the R_f selection method. This method is considered relevant due to diode current value at higher frequency (i.e: 300 *k*Hz) is becoming stable regardless of the change of the R_f value (refer to diode current of Figure 3 of [14] for R_d=10 *k*Ω and C_d=0.01 μF). Same principle applied to any components value at higher frequency, such as when R_d=10 *k*Ω and C_d=0.1 μF of Figure 2 of [14].

Figure 7 shows the linearity result using ΔC_x=0.1 *p*F change with R_d=10 *k*Ω and C_d=0.1 μF. Different R_f has been selected to overcome the sensitivity problems where Figure 7 is at R_f=200 *k*Ω at f_{ext}=300 *k*Hz. These values must satisfy the condition > f_{-3dB} range. In this case the frequencies are 3.183 *k*Hz, 159 *k*Hz and 106 *k*Hz respectively, when f_{-3dB}=159.13 Hz. At high frequency, high sensitivity of capacitive change of detection is achieved by reducing the value of the feedback resistor R_f,

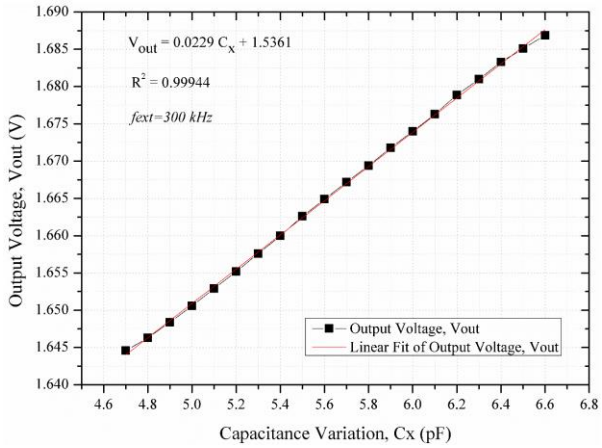

Figure 7. Corrected capacitance change, ΔC_x=0.1 *p*F with R_f=200 *k*Ω at f_{ext}=300 *k*Hz

3.2. Simulation with parasitic capacitance and resistance integration

In this test, parasitic capacitance and resistance involved in the real situation is mimicked as in the Z_{sense} part of circuit in Figure 1 under parasitic capacitance and resistance region. This is done by using the component's value tested earlier, R_f=10 *M*Ω, C_f=5 *p*F, R_d=10 *k*Ω, C_d=0.1 μF, V_s=3.3 V, C_r=5 *p*F, C_x=0.1-12

*p*F, and by including the parasitic components, R_A=2.2 Ω, R_P=30 *M*Ω, C_{p3}=0.05 *p*F, C_{p1}=0.56 *p*F, C_{p2}=0.56 *p*F for comparison purpose. Figure 8 shows the results using 300 *k*Hz frequency. The 300 *k*Hz frequency was chosen to test the possibilities and condition of the differential amplifier when running at frequency higher than 100 *k*Hz.

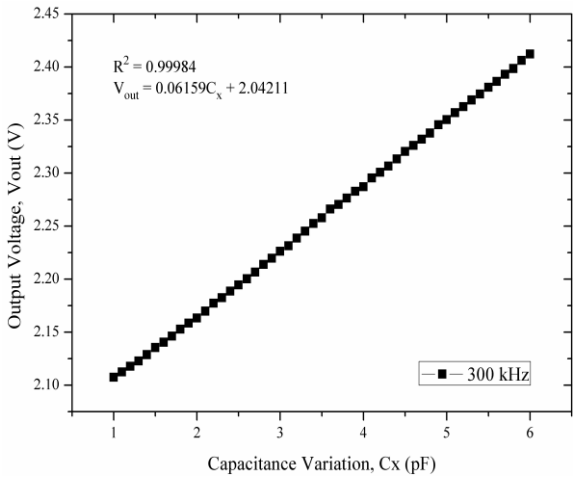

Figure 8. Corrected capacitance change, ΔC_x=0.1 *p*F with R_f=200 *k*Ω at f_{ext}=300 *k*Hz

Table 1 shows the results with and without parasitic condition at 300 *k*Hz excitation frequency. As predicted, the power consumption is higher with parasitic resistance and capacitance load. However, the output voltage range is higher with parasitic.

Table 1. Different simulation result using R_d=10 *k*Ω and C_d=0.1 μF when excitation frequency, f_{ext}=300 *k*Hz with and without parasitic resistance and capacitance exist

Test	Detection range, C_x (*p*F)	Output Voltage (V)	P_{diss} (*m*W)	Sensitivity (*m*V/*f*F)	R-squared value
With Parasitic	1.0 – 6.0	2.1075 – 2.4122	78.5	0.06094	0.99984
Without Parasitic	4.7 – 6.6	1.6446 – 1.6869	3.83	0.02226	0.99944

It is observed from the simulation result; power dissipation is increased when parasitic is included in the design. This is due to the high resistance involved across the capacitance detection sensor, C_x (i.e: R_P=30 *M*Ω). Therefore, more energy is needed for the operation. As a result, the DC output voltage range has also increased in the system. Proper measurement is required to obtain these stray resistances and capacitances value, but absolute values are impossible to be measured in real situation. Precaution is done to avoid unnecessary error and is according to the minimal value of *p*F range stated in [10], so that the parasitic value is not affected the C_x value. For example, when the parasitic across the C_x is chosen to be $1/100$ of the C_x, (i.e: $C_{p3=}$0.05 *p*F). Results have shown a wider detection range with increasing in sensitivity. In contra, power dissipation has also increased. These analyses and results were supported in [15].

4. CONCLUSION

In summary, this work has shown a proposed differential capacitive sensing with parasitic impedance. It is important to integrate the real situation into design consideration. Result has shown an increase of power dissipation to the system. A small increasing of 0.03868 *m*V/*f*F and 0.99984 were shown for sensitivity and R-squared values respectively at the output voltage, with parasitic components integration. The capacitance detection range is 1.0 – 6.0 *p*F. In future, a proposed solution can be done to improve points of detection of output voltage capacitance sensing across frequencies, by properly setting the values of component involved such as resistance and capacitance of the differential capacitive sensing.

ACKNOWLEDGEMENTS

This work is funded by the Research Initiative Grant Scheme (RIGS)-2018 (Ref: IIUM/504/G/14/3/1/1/RIGS17-023-0598) by the Research Management Centre, International Islamic University Malaysia.

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BIOGRAPHIES OF AUTHORS

Nurul Arfah Che Mustapha received the B. Eng. Electronics-Computer and Information Engineering and M. Sc. (Electronics Engineering) from the International Islamic University Malaysia (IIUM), Malaysia in 2008 and 2011, respectively. She obtained her Ph.D. degree in Electronics Engineering from IIUM in 2017. She was a graduate research assistant from 2009-2016 and received IIUM Fellowship from 2011-2015 for her Ph.D degree. Currently, Nurul Arfah works as a Asst. Prof. at the Electrical and Computer Engineering Department, Kulliyyah of Engineering, International Islamic University Malaysia (IIUM). Her research interest is in CMOS, VLSI circuit design, Energy Harvesting and Wireless Sensor Networks, and signal processing of capacitive sensor. Nurul Arfah is also a graduate member of the Instituition of Engineers Malaysia since March 2018 and Member of Institute of Electrical and Electronic Engineers (IEEE), M'18, since early 2018.

AHM Zahirul Alam works as a Professor at the Department of Electrical and Computer Engineering, International Islamic University Malaysia. Prof. AHM Zahirul Alam received his Doctorate of Engg. at Kanazawa University, Japan in March 1996. He did his M.Sc. Engg. in Electrical and Electronic Engineering and B.Sc. Engg. Electrical and Electronic Engineering, in Bangladesh University of Engineering and Technology (BUET) in Bangladesh, both on July 1987 and August 1984, respectively. His research interest is in Solid state devices modeling and characterizations, Microelectronic circuit design, VLSI circuit design, RF CMOS and RF MEMS, Antenna design, Energy Harvesting and Wireless Sensor Networks, Fabrication processes and material characterizations by XRD, FTIR, Raman Spectroscopy, AFM, TEM/SEM. Prof. AHM Zahirul Alam also a Chartered Engineer member of Engineering Council, UK on Nov 2016. Other professional background includes: Life Fellow of Institution of Engineers, Bangladesh (IEB, Bangladesh), since 2006, Life Fellow, Bangladesh Computer Society, since 2005, Senior Member of Institute of Electrical and Electronic Engineers (IEEE), M'90, SM'06 (Sept 23, 2006), Member of Institution of Engineering and Technology, IET since December 2015, Member of Institute of Electronics, Information and Communication Engineers, IEICE, Japan, since 2007, Member of International Association of Engineers, IAENG since 2016, Member of IEEE Electronic Devices Society, Member of IEEE Instrument and Measurement Society and Founder Member of Bangladesh Electronics Society since 1999.

Sheroz Khan received the B.Sc. degree in Electrical and Electronic Engineering from the N-W.F.P University of Engineering and Technology (NWFP UET), Peshawar, Pakistan. He obtained MSc degree in Microelectronic & Computer Engineering in 1990 from the University of Surrey, UK. He obtained PhD in Electrical Engineering in 1994 from University of Strathclyde, UK. He remained a faculty member within the department of Electrical and Electronic Engineering at the NWFP UET Peshawar until December 1999 until he joined UNITEN as a Principal Lecture in January 2000. He is senior member of the IEEE and ahs his research interests in power electronics, instrumentation and measurement, smart interfaces and biomedical electronics engineering. He has authored two books and over 100 articles in journals and in the IEEE Proceedings. Dr. Sheroz Khan also a Chartered Engineer member of Engineering Council, UK.

Amelia Wong Azman (M'06) received the B. Eng. Electronics from the University of Southampton, United Kingdom in 2004 and a Ph.D. degree in 2011 from the University of Queensland, Australia. She was a graduate research assistant for the National ICT Australia (NICTA) from 2006-2010 working with a team on smart surveillance project. Currently she is a lecturer in the Electrical and Computer Engineering Department, Faculty of Engineering, International Islamic University Malaysia (IIUM). Her research works are mostly in the area of VLSI design, signal processing and rehabilitation engineering.