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Design of Filter Using MOS Current Mode Logic

J Princy Joice*[1], M Anitha[2], I Rexlin Sheeba[3]
Dept of ECE Sathyabama University Chennai, Tamilnadu, India
*Corresponding authors, e-mail: princyjoice15@gmail.com, anita_velmurugan@yahoo.com, sheebarexlin@gmail.com

Abstract

MCML (MOS Current Mode Logic) is a method used for the purpose of reducing the delay and power of the circuit. In high speed application this method is used to reduce the power. In this method the sleep transistor is inserted in series with the supply voltage (or) current source to reduce the power. Different power gating techniques are been used to reduce the static power and to improve the speed and efficiency of the circuit. In this paper, the filter can be designed by using MCML logic. The fourth order band pass filter by using MCML logic is introduced. In order to reduce the power and delay this method is proposed.

Keywords*: MOS, current mode logic, MCML, filter, VLSI*

1. Introduction

The VLSI design is mainly based on less area, speed of the circuit, low power and low cost. In order to achieve these requirements, simple process, small area, small signal swings and low voltage circuits are needed. Most of these goals can be obtained from improving process technology, such as shrinking devices. The static CMOS design style is adopted in almost all digital applications. Such a wide spread diffusion is mainly due to its robustness and the negligible static power consumption. There are the specific requirements which cannot be fulfilled by static CMOS [1-5].

MCML logic is mainly used for digital application. A logic style that is becoming increasingly popular is MOS Current Mode Logic (MCML). This technique could be used to realize high-speed circuits. MCML has large static consumption due to its constant operation current. Its high-speed switching and reduced output voltage swing contribute to its high-performance. MCML having low switching noise because it's adapted in the mixed signal ICs to avoid the degradation of resolution. The advantage of this technique is that their speed and power consumption can be simply adjusted by altering the bias current of the gates without the need for resizing the devices. The near constant current of MCML produces significantly less on-chip simultaneous switching noise. This technique exhibits better power delay than the traditional CMOS logic style at high frequencies. MCML is preferred for mixed analogue-digital signal environments in order to reduce the digital interferences between the analogue and digital blocks. MCML architecture provide higher immunity to supply noise due to their differential structure, lower cross talk due to the reduced output voltage swing and lower noise generated due to the constant current flowing through the supply rails. Power dissipation of MCML circuits is much larger than the conventional CMOS at low operating frequency [1-5].

MCML circuits is used realize the high speed circuits. Based on the power the security key is fixed for the individual circuits. This method is used to secure the electronic data [1]. The PG-MCML consumes three times less power than the CMOS. It does not introduce the negative effect on robustness against power analysis attacks. The important goal of this method is minimizing the power, cost and battery life [2, 3]. MCML Multiplier based algorithm is used to get the high performance circuit. Transistor size is reduced in this method. The area of the circuit is also reduced in this method [6]. The power dissipation of the basic SRMCML cells are compared with the conventional dual-rail MCML. The power dissipation of the proposed SRMCML circuit is almost the same as the conventional dual-rail. The SRMCML circuit can attain smaller power delay product than dual-rail MCML [7]. 6T SRAM cells using MCML technology which will reduce the leakage power in SRAM cell and it will control the sub-

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threshold current [8]. In ring oscillator MCML logic is used. MCML ring oscillator consumes less power. Static power dissipation of the circuit is reduced because of its low voltage [9].

This paper addresses the design of filter using MCML logic. The MCML inverter circuit is inserted in the forth order band pass filter. The delay and power of the circuit is reduced using this method. This paper organized as follows. In section 2 describes the basic MCML logic. Section 3 focuses on the filter implementation of MCML logic. The results can be described in the section 4.

2. MCML Operating Principle

The MCML gate consists of four main blocks, (i.e) the logic function block, current source Ics, power switch, and the load resistors RL. Differential pair of NMOS transistors is used to implement the logic function. Depending on the complexity of the function levels, the NMOS transistors have to be stacked one upon the other to implement the logic function. The constant tail current Iss is provided by using a current source. This current will be switched based on the logic function to one of the output branch, which finally reach voltage level (Vdd-IssRd), which corresponds to logic '0' due to the entire current flowing through the load resistor. The other output will stay at logic '1'. The operation is elaborate in the next section. During *sleep* mode the power switch is used to cut the current, which will force both the outputs to logic '1', since there will be no current in the output branch.

In this MCML circuit (Figure 1), the design parameters include the voltage gain, total power dissipation, circuit delay and voltage swing. These parameters can be controlled by the variables such as bias current, current source transistor size, differential pull-down network transistor sizes, and the current source bias voltage.

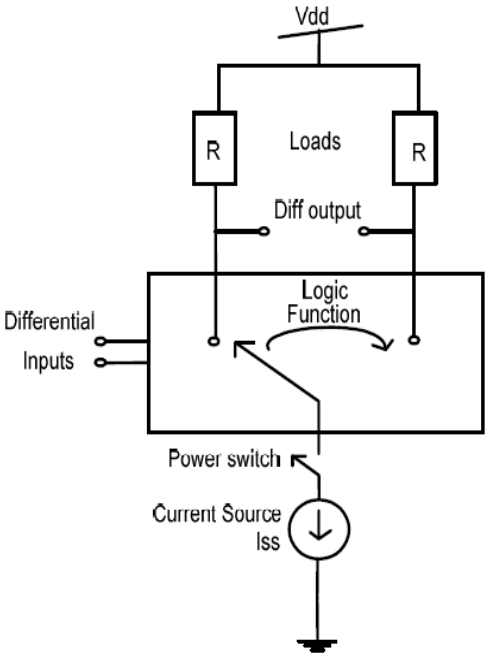

Figure 1. Basic MCML logic circuit

2.1 MCML Inverter

MCML circuit Figure 2 is having differential logic style with differential output and input. A standard NMOS differential pair is controlled by the single input. It is implemented in a pull down network switch. MCML circuits having two control voltages RFP and RFN. The NMOS current source gate voltage is declared by using RFN and it is used to determine the current value. The NMOS device of the current source has larger than minimum length. This is to

provide the higher output impedance for the current source and to reduce the effects of transistor length mismatch between the biasing and logic circuits. RFP determines the equivalent resistance of the PMOS load devices.

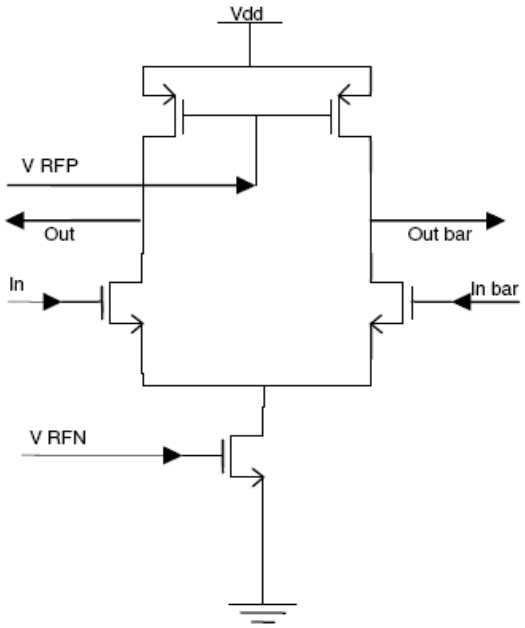

Figure 2. MCML Inverter

2.2 Modified MCML Inverter

In Figure 3 shows the modified MCML inverter. The sleep transistor is inserted in this method. This sleep transistor is used to reduce the power. V_RFN is acting as a current source of the device. This circuit realizes current to voltage conversion. A sleep transistor can be either a NMOS or PMOS transistor. The PMOS sleep transistor is declared as a *header switch* and it controls the supply voltage.

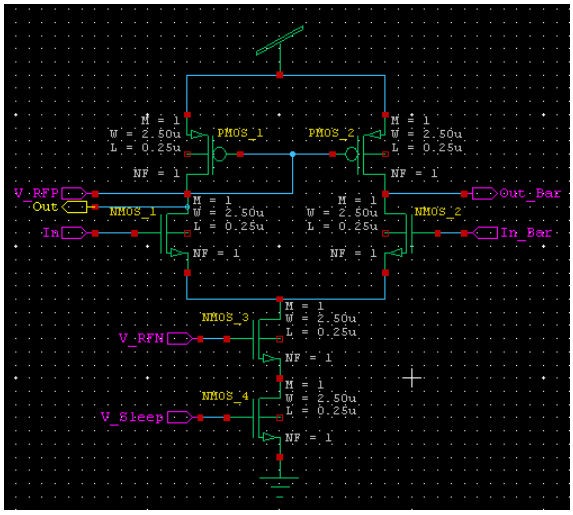

Figure 3. Modified MCML Inverter

The NMOS sleep transistor is declared as a *footer switch* and it controls the ground node connectivity. This sleep transistor is used to reduce the static power dissipation of the circuit. In order to reduce the power and delay this technique has been used. Based on the sleep transistor biasing the operation is performed. The performance of the circuit is increased and the efficiency is also increased. The delay value must be reduced by using this method.

3. Filter Implementation

The inverter stages are identical and it is used to invert the signals. For optimal accuracy the center frequency is controlled by an external clock. Two inputs are available for TTL or CMOS clock signals. The TTL input will accept logic levels referenced to the negative power supply pin or the ground pin, allowing operation on single or split power supplies. The CMOS input is Schmitt inverters which can be made to self oscillate using an external resistor and capacitor. TTL level shifter is used to shifting the level of the input signal. A level shifter is usually a part that converts digital signals from one logic standard to another. It might also be called a translator. A level shifter is used between digital circuits in order to convert “high” and “low” as used by one of the circuits into “high” and “low” as used by the other Figure 4.

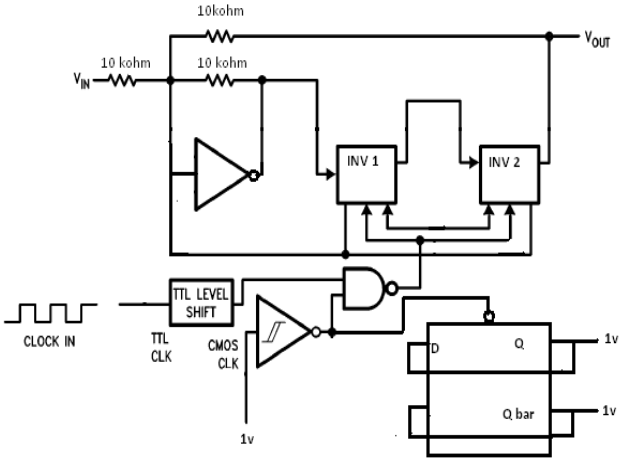

Figure 4. Fourth order band pass filter

The D type flip-flop has one data input ‘D’ and a clock input. The D flip-flop tracks the input, making transitions with match those of the input D. The circuit edge triggers on the clock input. The flip-flop also has two outputs Q and Q bar. Where Q bar is reverse of Q. Any input appearing (present state) at the input D, will be produced at the output Q in time T+1. If the present state we have D=0 and Q=1, the next state will be D=anything and Q=0. The output of the CMOS clock inverter and the TTL level shifter is connected to the NAND gate. The inverter is connected in the feedback loop. The D flip-flop clock signal is connected to the NAND gate. This signal is given to the input of the NAND gate. Instead of INV 1 and INV 2 the MCML inverter is replaced. In order to reduce the power of the circuit this MCML inverter is inserted in this circuit. Circuit performance is increased by using this method.

4. Result and Discussion

In this paper, the MCML based filter has been designed. Using this logic the circuit power and delay is reduced. Based on these performances the normal inverter circuit, MCML inverter circuit, modified MCML inverter circuit and the filter circuit are compared. The MCML filter has the better results compared to the normal filter. This filter has better performances.

Normal inverter simulation output is as shown in Figure 5.

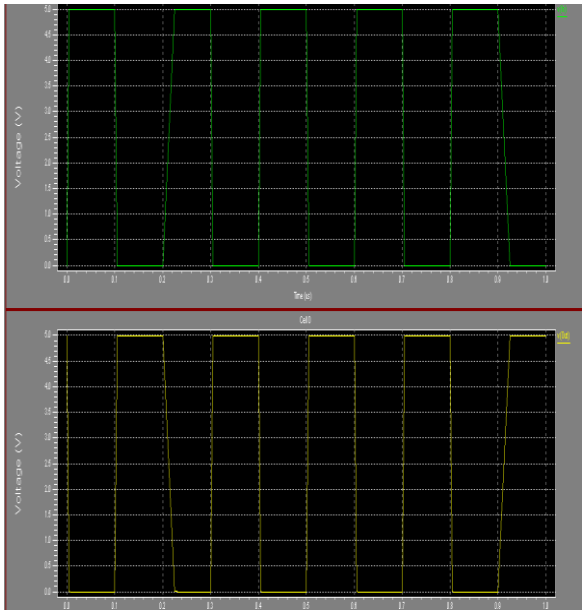

Figure 5. Normal inverter simulation output

MCML inverter simulation output is as shown in Figure 6.

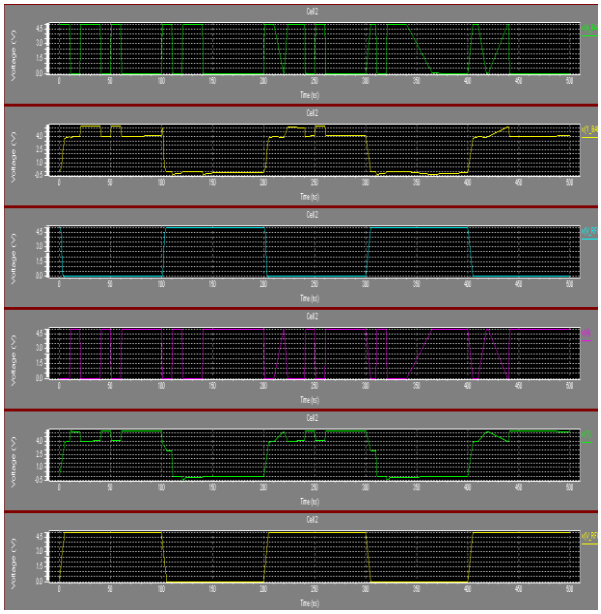

Figure 6. MCML inverter simulation output

Modified MCML inverter simulation output is as shown in Figure 7.

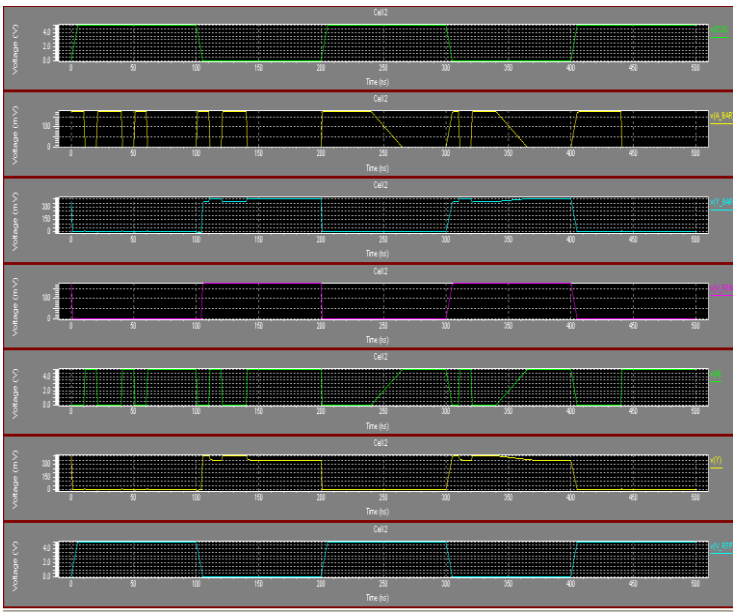

Figure 7. Modified MCML inverter simulation output

Filter circuit simulation output is as shown in Figure 8.

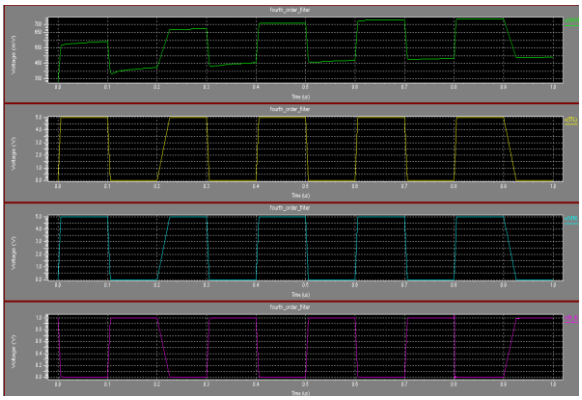

Figure 8. Filter circuit simulation output

The comparison performance of the above filters is shown in Table 1.

Table 1. Comparision of the filters

	POWER	DELAY
Inverter	5.750083e-015 watts	6.4823-012
MCML inverter	4.076429e-015 watts	5.2501-011
Modified MCML inverter	1.019917e-012 watts	3.0211-015
Filter with modified MCML inverter	1.998297e-011 watts	3.5211-012

5. Conclusion

In this paper we present a MCML based 4th order band pass filter has been designed. In this method the sleep transistor is inserted in series with the supply voltage (or) current source to reduce the power. The MCML inverter is inserted in the filter block. In order to reduce the power and delay this method is proposed. The static power dissipation is also reduced in this method. The circuit performance is also increased and the efficiency of the circuit is increased. The operation speed also increased in this method. In future work, we are going to implement this modified inverter into the oscillator circuits.

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