

Substrate Current Evaluation for Lightly and Heavily Doped MOSFETs at 45 nm process Using Physical Models

Sanjay Sharma, R.P. Yadav, Vijay Janyani

Department of Electronics and Communication Engineering
Malaviya National Institute of Technology (M.N.I.T.), Jaipur, INDIA
e-mail: sharma@mnit.ac.in, rp.yadav@cimap.res, vijayjanyani@gmail.com

Abstract

Substrate noise is a major integration issue in mixed signal circuits; particularly at radio frequency (RF) it becomes a key issue. In deep sub micron MOSFETs hot carrier effect induces device degradation. The impact ionization phenomenon is one of the main hot carrier effects. The paper covers the process and device level simulation of MOSFETs by TCAD and the substrate current comparison in lightly and heavily doped MOS. PMOS and NMOS devices are virtually fabricated with the help of ATHENA process simulator. The modeled devices include the hot carrier effects. The MOS devices are implemented on lightly and heavily doped substrates and substrate current is evaluated and compared with the help of ATLAS device simulator. Substrate current is better in lightly doped substrate than in heavily doped one. Drain current is also better in lightly doped than heavily doped substrates. Silvaco TCAD Tool is used for Virtual fabrication and simulation. ATHENA process simulator is used for virtual fabrication and ATLAS device simulator is used for device characterization.

Keywords: Substrate current, ATLAS, lightly and heavily doped substrate, impact ionization

1. Introduction

In sub-micrometer region substrate noise is of greater concern [1]. Substrate coupling in mixed signal circuits is an unavoidable and unintentional phenomenon. Any switching activity on digital part propagates to the analog by this substrate coupling, thus degrading the mixed signal circuit [2]. As the device is scaled down, hot carrier effect due to impact ionization causes reliability concern in devices and circuits [3] [4]. The resultant leakage current is studied in terms of substrate current, which constitute the substrate noise. Three broader areas are there in terms of substrate noise: noise generation, transmission and reception [5]-[7]. The substrate noise generation is a vital issue as the device scales down and is addressed in the form of hot carrier effects [8] [9]. The impact ionization because of hot carrier effect can be accounted as substrate current in circuit simulators to assess the performance degradation at the circuit level due to drift in the parameters of device. Mainly in a mixed signal circuit, device level noise cumulates to degrade the overall circuit. With the ATHENA process simulator, 45nm technology devices are fabricated in this paper, further substrate current is evaluated using ATLAS device simulator. This paper reveals that lightly doped substrate is better in comparison to heavily doped substrate in terms of noise coupling as lightly doped substrate has high resistivity than heavily doped substrate. The substrate current is evaluated with respect to the gate voltage and the drain voltage, for the four devices (lightly and heavily doped PMOS and NMOS). The results validate that substrate coupling is less in lightly doped substrate than in heavily doped substrate. Section (II) describes the models used to account for the generation of the substrate current in NMOS and PMOS. Section (III) provides the description and the measurement of the device under test. In Section (IV) results are discussed. Section (V) provides Conclusion.

2. Modeling Substrate Current Generation

At sub-micrometer design substrate current evolves as prime leakage component. The following models from ATLAS [12] are used to model devices for substrate current generation and evaluation, matching the design geometries:

- (a) **Transport model:** For deep sub-micron devices energy balance transport model is used. In this model the carrier mobility is related to carrier energy. The model finally converges to high field saturated velocity limit, thus defining velocity saturation phenomena. The model is based on the derivations by Stratton [13] [14], using the Boltzmann transport equation as key equation. The energy balance transport model improves the simulation by implementing ionization models. Hot carrier transport equations are activated using this model, thus accounting for hot carrier effects.
- (b) **Tunneling model:** This model accounts for the tunneling of carriers from channel to gate through gate dielectric, this model accounts for carrier injection. Lucky hot carrier injection model is used, accounting for injected gate current.
- (c) **Mobility model :** Lombardi model is incorporated to account for the temperature, transverse field and doping dependencies of mobility [15]
- (d) **Generation recombination model:** Particularly Shockley-Read-Hall (SRH) concentration dependent lifetime model is used. Carrier lifetime is made function of impurity concentration
- (e) **Impact model:** Selberherr's impact ionization model is used. The model accounts for impact ionization, key phenomena at RF, local electric field and temperature are accounted by it.

Out of the models used, Impact ionization is the main model [16] for substrate current evaluation [17]. At higher frequency impact ionization becomes vital phenomena for device level noise.

3. Process and Device Simulation

Virtual fabrication of NMOS and PMOS is done with ATHENA at 45 nm technology. Device physics is involved in modeling the devices, particularly at submicron technology it plays important role. Device physics helps us to link device noise with substrate noise. Substrate noise is modeled as the sum of microscopic noise and local noise. With a decrease in channel length, impact ionization and subsequently substrate current increases [18]. The Four devices are virtually fabricated, i.e., lightly and heavily doped NMOS, lightly and heavily doped PMOS. The device width is 1 μ m. Impact ionization model is applied to all the four modeled devices for better substrate current generation and extraction. The process steps for the devices are taken from Table 1 and Table 2:

Table 1. NMOS Process sheet

Process	Lightly doped NMOS	Heavily doped NMOS
Initial substrate	P-Type-1e15	P-Type-1e18
P well implant	Boron dose 1e12/cm ²	Boron dose 1e12/cm ²
Gate oxide thickness	1nm	1nm
V _i implant	Boron=1.5e13	Boron=1.5e13
Poly deposition	80nm	80nm
S/D implant	Arsenic=1e15	Arsenic=1e15
Halo implant	Boron 5e13	Boron 5e13
	Energy 25	Energy 25
	Angle 30 ^o full rotation	Angle 30 ^o full rotation
S/D implant (deep)	3e15, 7.5Kev	3e15, 7.5keV
RT Annealing	750-800 nitro for 1 min.	750-800 nitro for 1 min.
Metal deposition	Al-10nm	Al-10nm

Table 2. PMOS Process sheet

Process	Lightly doped PMOS	Heavily doped PMOS
Initial substrate(Si)	n-type-1e15	n-Type-1e18
n well implant	Phosphorous dose=7e13/ cm ²	Phosphorous dose=7e13/ cm ²
Gate oxide thickness	1nm	1nm
V _i implant	Arsenic 5e12	Arsenic 5e12
Poly deposition	80nm	80nm
S/D implant	Boron 1.5e14	Boron 1.5e14
Halo implant	Arsenic 1.5e13	Arsenic 1.5e13
	Energy 20	Energy 20
	Angle 35 ^o full rotation	Angle 35 ^o full rotation
S/D implant (deep)	1.5e15, 3Kev	1.5e15, 3Kev
RT Annealing	750-800 nitro for 1 min.	750-800 nitro for 1 min.
Metal deposition	Al-10nm	Al-10nm

The results of process simulator are used as input for device simulator and thus device characteristics are evaluated. In this way we can study the effect of process parameters on device performance and further device structure and fabrication process can be optimized. D.C. analysis is performed for all the four devices. Threshold voltage in saturation ($V_{t, \text{sat}}$) and in linear region ($V_{t, \text{lin}}$) is determined. To determine the current driving capability of the device I_{on} and I_{off} are calculated. SS (sat/lin) define slope in saturation and in linear region. Calculated Drain induced barrier lowering (DIBL) accounts to the short channel effects in MOSFETs. For all the four fabricated devices the above mentioned parameters are calculated using ATLAS (SILVACO). All the calculated parameters help us to check that whether or not our fabricated device is working well. The extracted device parameters for lightly and heavily doped NMOS are given in Table 3:

Table 3.

Parameters	Lightly doped NMOS	Heavily doped NMOS
$V_{t, \text{sat}}$	0.21164 V	0.224777 V
$V_{t, \text{lin}}$	0.253492 V	0.261598 V
SS sat	0.0777042 V/dec	0.0784734 V/dec
SS lin	0.0792496 V/dec	0.0798562 V/dec
DIBL	0.036393 V/V	0.0320183 V/V
I_{on}	0.00213986 A	0.00188337 A
I_{off}	3.79865e-09 A	2.69667e-09 A

Similarly for lightly and heavily doped PMOS the extracted device parameters are given in table 4:

Table 4.

Parameters	Lightly doped PMOS	Heavily doped PMOS
$V_{t, \text{sat}}$	-0.18089 V	-0.26236 V
$V_{t, \text{lin}}$	-0.277837 V	-0.348957 V
SS sat	0.0988542 V/dec	0.0706196 V/dec
SS lin	0.0722356 V/dec	0.0707719 V/dec
DIBL	-0.0843017 V/V	-0.0753017 V/V
I_{on}	-0.000818387 A	-0.000747102 A
I_{off}	-1.43462e-07 A	-4.74127e-10 A

4. Results

For all the four devices substrate current is Plotted against the gate and drain voltages. For Figure 1 I_d Vs V_d simulation has been done for lightly and heavily doped NMOS. Out of that substrate current (I_{Sub}) is extracted. During simulation we ramp our device from 0V to 1.2V for drain voltage, for different linear and saturation region gate voltages. For Figure 2 I_d Vs V_g simulation has been done for lightly and heavily doped NMOS. Similarly I_{Sub} (Substrate current) is extracted. During simulation we ramp our device from 0V to 1.2V for gate voltage, for different linear and saturation region drain voltages. From Figure 1 and Figure 2 Substrate current is more dominant in heavily doped NMOS than in lightly doped NMOS, the order of difference is almost one. These plots clearly depict that MOS with lightly doped substrate is better than heavily doped substrate in terms of substrate coupling. Substrate coupling is measured as the amount of substrate current that is further coined as substrate noise.

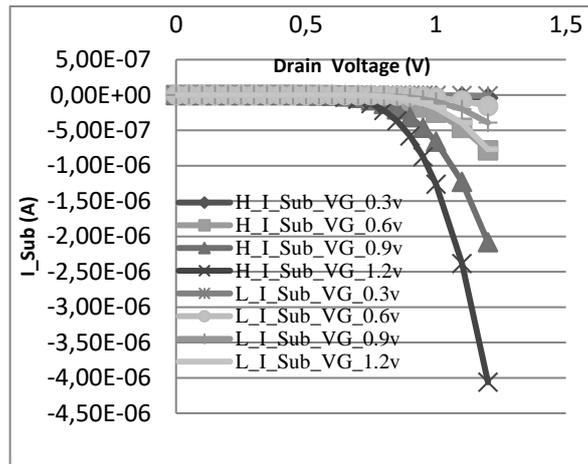


Figure 1. Comparison of Substrate current Vs Drain voltage for lightly and heavily doped substrate NMOS

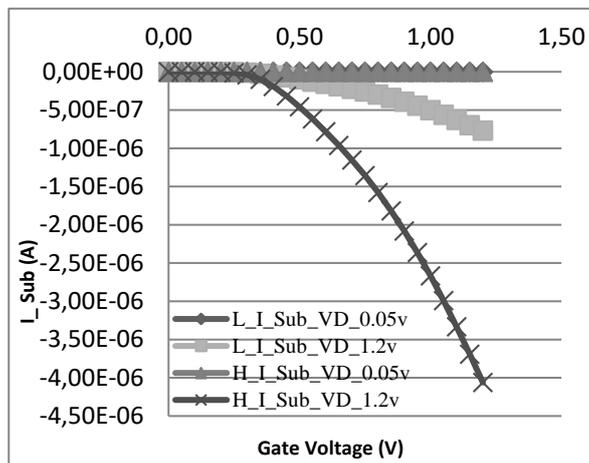


Figure 2. Comparison of Substrate current Vs Gate voltage for lightly and heavily doped substrate NMOS

Similar characteristics for PMOS are evaluated from Figure 3 and Figure 4. All the assumptions in the case of PMOS devices are just opposite to that in NMOS. In the case of PMOS also the lightly doped PMOS has less substrate current in comparison of heavily doped PMOS. For both the NMOS and PMOS devices impact ionization Phenomena is responsible for the better extraction of substrate current. This device level noise accumulates at circuit level to degrade the circuit performance.

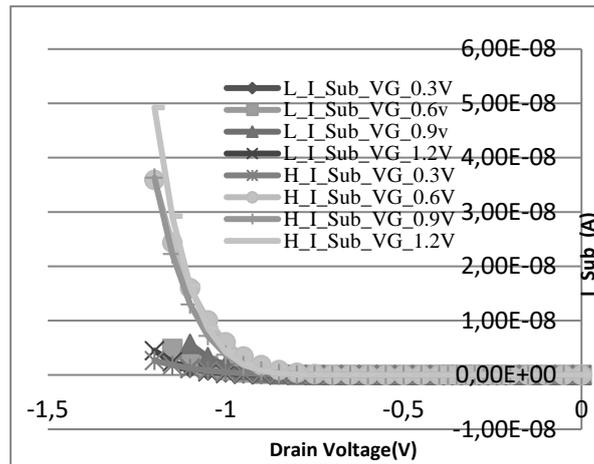


Figure 3. Comparison of Substrate current Vs Drain voltage for lightly and heavily doped substrate PMOS

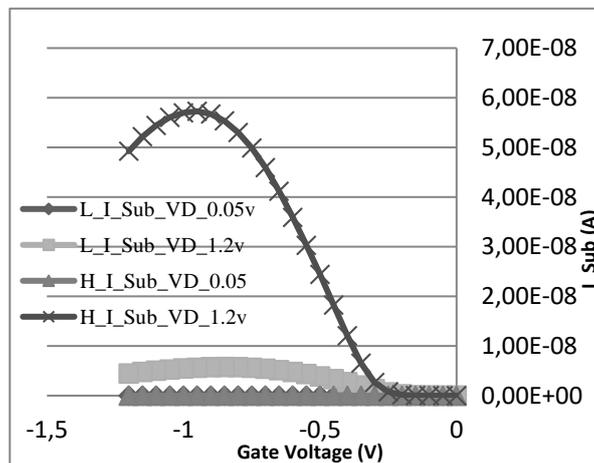


Figure 4. Comparison of Substrate current Vs Gate voltage for lightly and heavily doped substrate PMOS

5. Conclusion

Device level noise at sub micrometer design can lead to serious circuit integration issues. Four MOS devices are virtually fabricated and their characteristics are evaluated for substrate current for lightly and heavily doped substrate. Lightly doped substrate provides better noise immunity in comparison to heavily doped substrate. At 45nm technology node device modeling is performed for PMOS and NMOS with the help of ATLAS to validate the behavior of substrate. Substrate current for heavily and lightly doped substrates is evaluated for PMOS and NMOS devices. Substrate current is more pronounced in the case of heavily doped substrate, making it less suitable at device level. The substrate current in lightly doped substrate device is less than by more than an order when compared to heavily doped device. Therefore the lightly doped substrate devices provides better substrate noise immunity and devices fabricated on lightly doped substrate provides better drain characteristics than heavily doped substrate devices.

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